High-Speed USB Converter Chip CH347

Datasheet

Version: 1.4

https://wch-ic.com

1. Overview

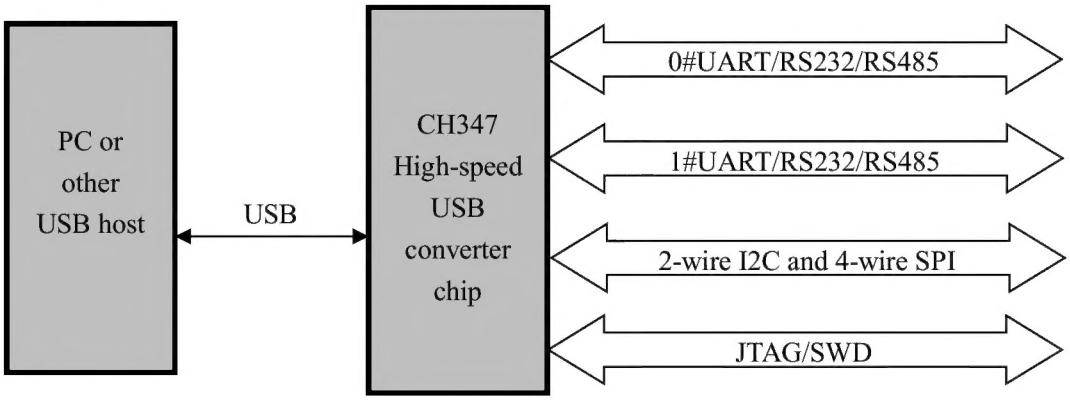
CH347 is a high-speed USB bus converter chip that provides UART, I2C and SPI synchronous serial interface and JTAG interface through USB bus.

In UART mode, CH347 provides 2 high-speed serial ports, supports RS485 UART transceiver enable control, hardware flow control, and common MODEM signals, used to extend serial ports for computer, or upgrade directly from normal serial devices or MCU to USB bus.

In synchronous serial interface mode, CH347 provides one 2-wire I2C interface (SCL, SDA) and one 4-wire SPI interface (SCS, SCK/CLK, MISO/SDI/DIN, MOSI/SDO/DOUT) to extend 2-wire or 4-wire synchronous serial port for computer to operate EEPROM, FLASH, sensors, etc.

In JTAG mode, CH347 provides one JTAG interface that supports either a 4/5/6-wire interface (TMS, TCK, TDI, TDO, TRST and SRST) for extending JTAG interface for computer to operate devices such as CPU, DSP, FPGA, and CPLD.

In the SWD mode, the CH347 provides one SWD interface (SWDCLK, SWDIO) for expanding the SWD interface for computers to operate devices such as ARM MCUs and CPUs.



2. Features

2.1 Introduction

- 480Mbps high-speed USB device interface, peripheral components only need crystal oscillator and capacitor.
- Built-in EEPROM with configurable parameters such as working mode, the chip of VID, PID, maximum current value, vendor and product information string.
- Support only 3.3V power supply voltage.
- CH347F supports I/O independent power supply with 3.3V, 2.5V, and 1.8V supply voltages.
- RoHS compliant TSSOP-20 and QFN28 lead free package.
- Multiple working modes, suitable for high-speed USB converter applications.

2.2 UART

- Built-in firmware, emulate standard UART interface, used to upgrade the original serial peripheral or expand additional UART via USB.
- Original serial applications are totally compatible without any modification in Windows operating system.
- Hardware full-duplex UART interface, integrated independent transmit-receive buffer, supports communication baud rate varies from 1200bps to 9Mbps.
- UART supports 5/6/7/8 data bits, no parity/odd parity/even parity/blank parity/flag parity, and 1/2 stop bits.
- Built-in 12K bytes RX-FIFO and 4K bytes TX-FIFO for each UART.
- Support common MODEM signals RTS, DTR, DCD, RI, DSR and CTS.
- Support CTS and RTS hardware automatic flow control.
- Support half-duplex, provides transmitting status TNOW which supports RS485 switching.
- Support up to 8-channel GPIO input and output function.
- Support RS232, RS485, RS422 interface, through external voltage converter chip.

2.3 I2C Synchronous Serial Interface

- Work in Host/Master Host mode.
- Provide SCL and SDA 2 signal lines, support multiple transmission speeds, transmission frequency up to 1MHz.
- With the cooperation of computer API, flexible operation of 2-wire interface A/D, D/A, EEPROM and sensor components.

2.4 SPI Synchronizes Serial Interface

- Work in Host/Master Host mode.
- Provide SCS, SCK/CLK, MISO/SDI/DIN, MOSI/SDO/DOUT four signal lines.
- Support 2 chip select signal lines and can operate two SPI interface devices by time-sharing.
- Support 8-bit/16-bit data structure, supports MSB and LSB transmission.
- Support SPI mode 0/1/2/3, and supports transmission frequency configuration up to 60MHz.
- Support hardware DMA sending and receiving.
- With the cooperation of computer API, flexible operation of FLASH, MCU, sensor and other components with 4-wire interface.

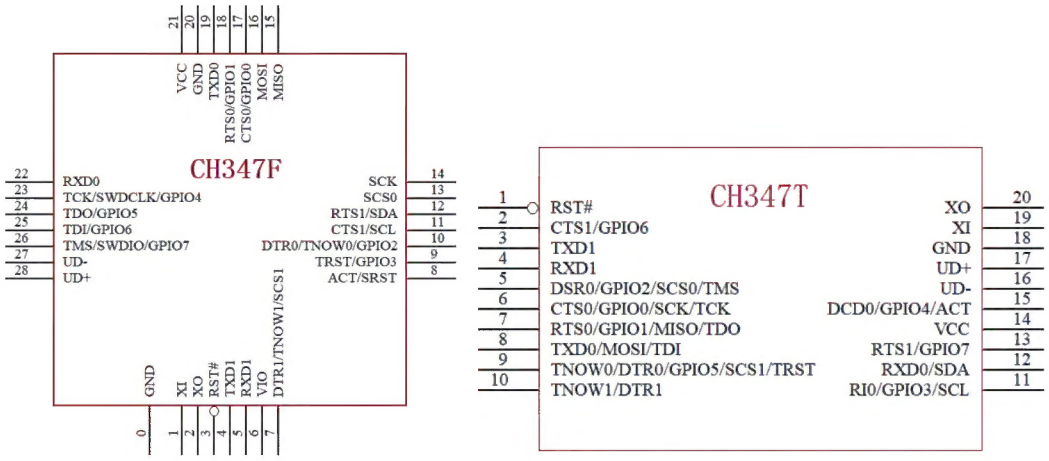
2.5 JTAG Interface

- Work in Host/Master Host mode.
- JTAG interface provides TMS, TCK, TDI, TDO, TRST (optional), and SRST (optional) cables.
- Support high-speed USB data transfer.
- With the cooperation of computer API, flexible operation of CPU, DSP, FPGA, CPLD, MCU and other components.

2.6 SWD Interface

- As Host/Master host mode.
- The SWD port provides SWDCLK and SWDIO cables.
- Through the cooperation of computer API, it can flexibly operate ARM MCU and CPU devices.

3. Pinouts



Package Form	Body Size	Pin Pitch		Package Description	Order Model
QFN28	4*4mm	0.4mm	15.7mil	Quad Flat No-Lead Package	CH347F
TSSOP20	4.4*6.5mm	0.65mm	25.6mil	Thin Shrink Small Outline Package	CH347T

Note: The USB transceiver of CH347 is fully built-in according to the USB2.0 design, and the UD+ and UD- pins cannot be connected to the resistor in series, otherwise the signal quality will be affected.

The EPAD of the CH347F is 0# pin GND, which is an optional but recommended connection; Other GND connections are required.

4. Pin Definitions

4.1 General Description

CH347 has multiple working modes, and the function and definition of the same pin in different working modes may be different. CH347T automatically configures the working mode by detecting the configuration pin status during power-up reset or external reset.

Note: FT indicates pin withstands 5V when used as an input.

4.2 CH347F Pins

Table 4-1 Standard common pins

Pin No.	Pin Name	Pin Type	Pin Description
21	VCC	P	Power supply voltage input, requires an external decoupling capacitor
0/20	GND	P	Ground, connected to ground of USB bus directly
3	RST#	I	Input of external reset, active low, built-in pull-up resistor
28	UD+	USB	Connect to USB D+ Signal directly, do not connect resistor in series
27	UD-	USB	Connect to USB D- Signal directly, do not connect resistor in series
1	XI	I	Input of crystal oscillator
2	XO	O	Inverted output of crystal oscillator
6	VIO	P	The power input of the I/O port requires an external decoupling capacitor decoupling capacitor

Table 4-2 SPI related pins

Pin No.	Pin Name	Pin Type	Pin Description
13	SCS0	O	The chip selection output of the 4-wire serial port is 0
7	SCS1	O	The chip selection output of the 4-wire serial port is 1
14	SCK	O	Clock output of 4-wire serial port, alias DCK
15	MISO	I(FT)	Data input of 4-wire serial port, alias DIN or SDI, built-in pull-up resistor
16	MOSI	O	Data output of 4-wire serial port, alias DOUT or SDO

Table 4-3 JTAG related pins

Pin No.	Pin Name	Pin Type	Pin Description

25	TDI	O	Data output of the JTAG interface
24	TDO	I(FT)	Data input of the JTAG interface, built-in pull-up resistor
23	TCK	O	Clock output of the JTAG interface
26	TMS	O	Mode selection of the JTAG interface
9	TRST	O	Reset output of the JTAG interface
8	SRST	O	System reset output of the JTAG interface

Table 4-4 SWD related pins

Pin No.	Pin Name	Pin Type	Pin Description
23	SWDCLK	O	Clock pin of the SWD interface
26	SWDIO	I/O (FT)	Data pin of the SWD interface

Table 4-5 I2C interface related pins

Pin No.	Pin Name	Pin Type	Pin Description
12	SDA	I/O	Data input and output of 2-wire serial port
11	SCL	O	Clock output of 2-wire serial port

Table 4-6 UART related pins

Pin No.	Pin Name	Pin Type	Pin Description
19	TXD0	O	Serial data output of UART0, idle state is high level
22	RXD0	I(FT)	Serial data input of UART0, built-in pull-up resistor
4	TXD1	O	Serial data output of UART1, idle state is high level
5	RXD1	I	Serial data input of UART1, built-in pull-up resistor
17	CTS0	I (FT)	UART0 MODEM input signal, clear to transmit, active low;
18	RTS0	O	UART0 MODEM output signal, clear to transmit, active low; During power-on, if the RTS0 pin detects that the external pull-down resistor is connected, the configuration parameters in the internal EEPROM are disabled and the default parameters of the chip are enabled
11	CTS1	I (FT)	UART1 MODEM input signal, clear to transmit, active low;
12	RTS1	O	UART1 MODEM output signal, request to transmit, active low;
10	DTR0/TNOW0	O	UART0 MODEM output signal, data terminal ready, active low; RS485 transmit and receive control pins for UART0; During power-on, if the DTR0 pin detects an external pull-down resistor, DTR0 and DTR1 switch to the TNOW0 and TNOW1 functions, respectively

7	DTR1/TNOW1	O	UART1 MODEM output signal, data terminal ready, active low; RS485 transmit and receive control pins for UART1

Table 4-7 GPIO related pins

Pin No.	Pin Name	Pin Type	Pin Description
17	GPIO0	I/O (FT)	GPIO0, used for IO port input or output.
18	GPIO1	I/O (FT)	GPIO1, used for IO port input or output.
10	GPIO2	I/O	GPIO2, used for IO port input or output.
9	GPIO3	I/O	GPIO3, used for IO port input or output.
23	GPIO4	I/O (FT)	GPIO4, used for IO port input or output.
24	GPIO5	I/O (FT)	GPIO5, used for IO port input or output.
25	GPIO6	I/O (FT)	GPIO6, used for IO port input or output.
26	GPIO7	I/O (FT)	GPIO7, used for IO port input or output.

Note 1: The 17th and 18th pins of the CH347F are powered by VCC at a 3.3V signal level; The power supply for the other pins comes from the VIO and is the 3.3V/2.5/1.8V signal level matched by the VIO.

Note 2: Explanation of table abbreviations:

USB = USB signal pin;

I = Signal input;

O = Signal output;

P = Power supply or ground;

N = Empty;

FT = Tolerant 5V.

4.3 CH347T Pins

Table 4-8 Standard common pins

Pin No.	Pin Name	Pin Type	Pin Description
14	VCC	P	The positive power input of the power regulator requires an external decoupling capacitor
18	GND	P	The common ground terminal must be connected to the ground cable of the USB bus
1	RST#	I	External reset input, low active, built-in pull-up resistor
17	UD+	USB	D+ data cable directly connected to USB bus, no additional series resistor
16	UD-	USB	D-data cable directly connected to USB bus, no additional series resistor
19	XI	I	Crystal oscillation input
20	XO	O	Crystal oscillating inverting output

Table 4-9 Working Mode Configuration Pins

Pin No.	Pin Name	Pin Type	Pin Description
10	DTR1/TNOW1	I (FT)	MODE0 configuration pin 0 for working mode when the chip is reset. Used with MODE1 pin, built-in pull-up resistor
13	RTS1/GPIO7	I (FT)	MODE1 configuration pin 1 for working mode when the chip is reset. Used with MODE0 pin, built-in pull-up resistor

Table 4-10 Working Mode 0 Pins

Pin No.	Pin Name	Pin Type	Pin Description
8	TXD0	O	Transmit asynchronous data output of UART0, high when idle
12	RXD0	I (FT)	Receive asynchronous data input of UART0, built-in pull-up resistor
3	TXD1	O	Transmit asynchronous data output of UART1, high when idle
4	RXD1	I (FT)	Receive asynchronous data input of UART1, built-in pull-up resistor
9	DTR0/TNOW0 /GPIO5	I/O	MODEM output signal of UART0, data terminal ready, active low; RS485 transmit and receive control pin of UART0; General purpose GPIO5, used for IO input or output. During power-on, if DTR0 detects an external pull-down resistor, DTR0 and DTR1 switch to TNOW0 and TNOW1 respectively
10	DTR1/TNOW1	O	MODEM output signal of UART1, data terminal ready, active low; RS485 transmit and receive control pin of UART1
6	CTS0/GPIO0	I/O (FT)	MODEM input signal for UART0, clear to transmit, active low; General GPIO0, used for IO port input or output

7	RTS0/GPIO1	I/O	MODEM output signal of UART0, request to transmit, active low; General GPIO1, used for IO port input or output. During power-on, if RTS0 detects an external pull-down resistor, disable the configuration parameters in the internal EEPROM and enable the default parameters delivered with the chip
2	CTS1/GPIO6	I/O (FT)	MODEM input signal of UART1, clear to transmit, active low; General GPIO6, used for IO port input or output
13	RTS1/GPIO7	I/O	MODEM output signal of UART1, request to transmit, active low; General GPIO7, used for IO port input or output
11	RI0/GPIO3	I/O (FT)	MODEM input signal for UART0, ring indicator, active low; General GPIO3, used for IO port input or output
15	DCD0/GPIO4	I/O (FT)	MODEM input signal for UART0, data carrier detect, active low; General GPIO4, used for IO port input or output
5	DSR0/GPIO2	I/O (FT)	MODEM input signal of UART0, data set ready, active low; General GPIO2, used for IO port input or output

Table 4-11 Working Mode 1/2 Pins

Pin No.	Pin Name	Pin Type	Pin Description
3	TXD1	O	Transmit asynchronous data output of UART1, idle state is high level
4	RXD1	I (FT)	Receive asynchronous data input of UART1, built-in pull-up resistor
10	DTR1/TNOW1	O	MODEM output signal of UART1, data terminal ready, active low; RS485 transmit and receive control pin of UART1
2	CTS1	I (FT)	MODEM input signal of UART1, clear to transmit, active low
13	RTS1	O	MODEM output signal of UART1, requests to transmit, active low

7	MISO	I (FT)	4-wire serial port data input, alias DIN or SDI, built-in pull-up resistor
8	MOSI	O	4-wire serial port data output, alias DOUT or SDO
6	SCK	O	4-wire serial port clock output, alias DCK
5	SCS0	O	4-wire serial port chip selection output 0
9	SCS1	O	4-wire serial port chip selection output 1
12	SDA	I/O (FT)	2-wire serial port data input and output, built-in pull-up resistor
11	SCL	O	2-wire serial port clock output, built-in pull-up resistor
15	ACT	O	USB configuration completed status output, active low During power-on, if the ACT pin detects an external pull-down resistor, DTR1 switches to the TNOW1 function

Table 4-12 Working Mode 3 Pins

Pin No.	Pin Name	Pin Type	Pin Description
3	TXD1	O	Transmit asynchronous data output of UART1, idle state is high level
4	RXD1	I (FT)	Receive asynchronous data input of UART1, built-in pull-up resistor
10	DTR1/TNOW1	O	MODEM output signal of UART1, data terminal ready, active low; RS485 transmit and receive control of UART1
2	CTS1	I (FT)	MODEM input signal of UART1, clear to transmit, active low
13	RTS1	O	MODEM output signal of UART1, requests to transmit, active low
8	TDI	O	Data output of JTAG interface
7	TDO	I (FT)	Data input of JTAG interface, built-in pull-up resistor
6	TCK	O	Clock output of JTAG interface
9	TRST	O	Reset output of JTAG interface
5	TMS	O	Mode selection of JTAG interface
11, 12	GPIO	I/O	General GPIO, used for IO port input or output
15	ACT	O	USB configuration completed status output, active low During power-on, if the ACT pin detects an external pull-down resistor, DTR1 switches to the TNOW1 function

Note 1: Explanation of table abbreviations:

USB = USB signal pin;

I = Signal input;

O = Signal output;

P = Power supply or ground;

N = Empty;

FT = Tolerant 5V.

5. Functional Description

5.1 General Description

CH347 is a high-speed USB bus converter chip that provides UART, common 2-wire I2C and 4-wire SPI synchronous serial interface, JTAG interface, etc.

VCC pin is the input of power supply, which requires 3.3V power supply voltage. The power pin VCC should be connected to an external power decoupling capacitor of about 0.1uF.

The VIO pin of the CH347F chip is used to provide I/O power to the I/O and RST pins, supporting 1.8V to 3.3V power supply voltage, and the VIO should use the same power supply as the MCU and other peripherals. The UD+ and UD- pins use VCC power, not VIO power. For CH347F chips with Lot 5 ≥ 4, VIO supports 1.2V supply voltage.

CH347 chip has a built-in power-on reset circuit. When the chip is operating, it needs to provide an external 8MHz clock signal to the XI pin. The clock signal can be generated by the built-in inverter of CH347 through crystal frequency stabilization oscillation. The peripheral circuit needs to connect an 8MHz crystal between the XI and XO pins, and the both pins connect to the ground with an oscillation capacitor of about 22pF.

CH347 has built-in all peripheral circuits required by the USB bus, including the embedded USB controller and USB-PHY, the series matching resistor of the USB signal wire, and the 1.5K pull-up resistor required for the Device. The UD+ and UD- pins should be connected directly to the USB bus.

5.2 Working Mode Configuration

The CH347F does not require a working mode and supports high-speed serial ports, I2C, SPI, JTAG, and SWD interfaces. The function of multiplexing pins can be switched and controlled by the driver.

Chip Function	Default Product ID
5-in-1: USB to high-speed dual serial port + USB to 2-wire I2C + USB to 4-wire SPI+ USB to JTAG interface + USB to SWD interface	55DEH

When CH347T is reset, the chip detects the level status of DTR1 (PIN10) and RTS1 (PIN13) pins. Chip working modes and their switching functions are described in the following table.

Working Mode	DTR1 and RTS1 Pin Status	Chip Function	Default Product ID
Mode 0	DTR1 is floating or high level, RTS1 is floating or high level	USB to high-speed dual UARTs. UART0 supports full MODEM signals, UART1 supports partial MODEM signals	55DAH
Mode 1	DTR1 is floating or high level, RTS1 is pulled down to low level	Vendor driver mode 3-in-1: USB to high-speed single UART + USB to 2-wire I2C + USB to 4-wire SPI	55DBH

Mode 2	DTR1 is pulled down to low level, RTS1 is floating or high level	HID Driver-free mode 3-in-1: USB to high-speed single UART + USB to 2-wire I2C + USB to 4-wire SPI	55DCH
Mode 3	DTR1 is pulled down to low level, RTS1 is pulled down to low level	2-in-1: USB to high-speed single UART + USB to JTAG interface	55DDH

Working Mode 0: USB to high-speed dual UARTs. On the computer, it will be recognized as two standard USB serial ports, suitable for the simultaneous use of dual UARTs requirements. UART0 supports full MODEM signals, and UART1 supports partial MODEM signals. Both UARTs support hardware flow control and RS485 serial port transmit/receive enable control.

Working Mode 1: Vendor driver mode 3-in-1, USB to high-speed single UART, USB to 2-wire I2C and USB to 4- wire SPI synchronous serial interface. On the computer, it will be recognized as a standard USB serial port and a custom interface for 2-wire and 4-wire synchronous serial interface communication, suitable for the simultaneous use of UART and 2-wire or 4-wire synchronous serial interface requirements. UART1 supports partial MODEM signals, hardware flow control, and RS485 serial port transmit/receive enable control. 4-wire synchronous serial interface supports configurations such as mode, data bits, and data sequence.

Working Mode 2: HID Driver-free mode 3-in-1, USB to high-speed single UART, USB to 2-wire I2C and USB to 4-wire SPI synchronous serial port. On the computer, it will be recognized as a class composite device with two customized HID interfaces (interface 0 is used for UART data upload and download, and interface 1 is used for 2-wire and 4-wire synchronous serial interface communication), suitable for the simultaneous use of UART and 2-wire or 4-wire synchronous serial interface, and it is not convenient to install the vendor's driver requirements. UART1 supports partial MODEM signals, hardware flow control, and RS485 serial port transmit/receive enable control. 4-wire synchronous serial interface supports mode (Mode 0/1/2/3), data bits (8-bit/16-bit), and data sequence (MSB/LSB).

Working Mode 3: 2-in-1, USB to high-speed single UART and USB to JTAG interface. On the computer, it will be recognized as one standard USB serial port and one JTAG interface, suitable for the simultaneous use of UART and JTAG interface requirements.

All operating modes of CH347F chip and CH347T chip support GPIO function and up to 8 channels of GPIO, which can be flexibly operated through the cooperation of computer API.

5.3 UART

CH347 provides one or two UART, each UART includes TXD, RXD, CTS, RTS, and DTR pin, etc. UART0 supports all MODEM signals, and UART1 supports partial MODEM signal lines.

In UART mode, CH347 contains: data transfer pins, MODEM interface signal pins and auxiliary pins.

Data transfer pins contain: TXD0, TXD1 and RXD0, RXD1. RXDx is high when UART transmission is idle. TXDx is high when UART reception is idle.

MODEM interface signal pins and RS485 transmit and receive control pins contain: CTS0, RTS0, DTR0, CTS1, RTS1, and DTR1.

The CH347 chip's serial port has a built-in independent transceiver buffer and supports simplex, half-duplex or full-duplex asynchronous serial communication.

The serial data of CH347 includes 1 low level start bit, 5/6/7/8 data bits, 1/2 high level stop bits, and supports no parity/odd parity/even parity/blank parity/flag parity. Supports common baud rate: 1200, 1800, 2400, 3600, 4800, 9600, 14400, 19200, 28800, 33600, 38400, 56000, 57600, 76800, 115200, 128000, 153600, 230400, 460800, 921600, 1M, 1.5M, 2M, 3M, 4M, 5M, 6M, 7M, 8M, 9M, etc. The CH347T chip supports up to 9M baud rate for the 2 serial ports in operating mode 0. In other operating modes, the serial port baud rate supports up to 7.5M by default.

Dual UARTs of CH347 both support CTSx and RTSx hardware automatic flow control which is not enabled by default, and can be enabled by VCP driver. If enabled, UART continues to transmit the next packet of data only when CTSx pin input is detected to be valid (active low), otherwise UART transmission is paused; UART automatically validates RTSx pin (active low) when the receive buffer is empty, invalidates RTSx pin until the receive buffer is nearly full, and then validates RTSx pin again when buffer is empty. With hardware automatic rate control, you can connect your CTSx pins to RTSx pins of the other side and your RTSx pins to CTSx pins of the other side.

The allowable baud rate error of CH347 UART receiving signal is not more than 4%, the baud rate error of UART transmitting signal is less than 1%.

In the Windows OS, after installing high-speed VCP vendor driver, it can emulate standard UART, so the mostly original serial applications are totally compatible, without any modification.

CH347 can be used to upgrade the original UART peripheral devices, or expand extra serial ports for computer via USB bus. Through external level conversion chip provides RS232, RS485, RS422 and other interface can be further.

5.4 I2C Synchronous Serial Interface

I2C/IIC synchronous serial interface of CH347 works in Host/Master host mode, includes SCL and SDA signal lines. SCL is used for unidirectional output synchronous clock, open-drain output, SDA is used for bidirectional data input and output, open-drain output and input.
The basic operation elements of I2C interface include: start bits, stop bits, bit output, and bit input.
Start bit is defined as SDA outputs falling edge when SCL is high level.
Stop bits is defined as SDA outputs rising edge when SCL is high level.
Bit output is defined as SDA outputs bit data when SCL is low level, and then SCL outputs high level pulse.
Bit input is defined as when SCL outputs high level pulse, SDA inputs bit data before falling edge.
I2C interface of CH347 supports multi-transmission speeds and can flexibly operate 2-wire A/D, D/A, EEPROM and sensor components with the cooperation of computer API.

5.5 SPI Synchronizes Serial Interface

4-wire SPI synchronous serial interface of CH347 works in Host/Master Host mode, includes four signal lines SCSx, SCK(CLK), MISO(SDI/DIN) and MOSI(SDO/DOUT). SCSx includes SCS0 and SCS1, which can operate

two SPI interface devices in time-sharing mode. Support 8-bit / 16-bit data structure, support MSB and LSB transmission, support SPI mode 0/1/2/3, support transmission frequency configuration, etc. Built-in hardware DMA, batch data can be quickly transmitted and read. With the cooperation of computer API, flexible operation of FLASH, MCU, sensor and other devices with 4-wire interface.

5.6 JTAG Interface

JTAG interface of CH347 works in Host/Master Host mode, includes six signal lines TMS, TCK, TDI, TDO, TRST and SRST. TRST and SRST is an optional signal line. Supports the fast mode and bit-bang mode of user-defined protocol, transmission rate up to 30Mbit/S.

Provide computer USB high-speed driver and USB to JTAG TAP function library, support secondary development, used to build customized USB to high-speed JTAG debugger, FPGA downloader, CPU programmer and other products.

5.7 SWD Interface

The SWD port of the CH347 chip works in Host or Master host mode. The SWD interface consists of two signal cables, SWDCLK and SWDIO.

Provide computer side USB high-speed driver and USB to SWD function library, support secondary development, used to build custom USB to SWD debugger, downloader and other products.

5.8 Chip Parameter Configuration

For larger volume applications, vendor identification code (VID) and product identification code (PID) and product information of CH347 can be customized.

For less volume applications, it can use the built-in EEPROM for parameter configuration. After user installs VCP vendor driver, through configuration tool CH34xSerCfg.exe provided by chip vendor, it can be flexibly configured the vendor identification code (VID), product identification code (PID), maximum current value, BCD version number, vendor information and product information string and other descriptor, etc.

6. Parameters

6.1 Absolute Maximum Ratings

Critical state or exceeding maximum value may cause the chip to work abnormally or even be damaged.

Name	Parameter Description	Min	Max	Unit
TA	Operating ambient temperature	-40	85	℃
TS	Storage ambient temperature	-40	125	℃
VCC	Supply voltage (VCC connects to power, GND to ground)	-0.3	4.0	V
VIO	I/O supply voltage (VIO pin supply, GND to ground)	-0.3	4.0	V
VUSB	USB signal voltage	-0.5	3.8	V
VIO5	Input voltage on the pin withstanding 5V	-0.5	5.6	V
VIO3	Input voltage on other pins	-0.5	VCC+0.3	V

6.2 Electrical Characteristics

Test conditions: TA=25℃, VCC=3.3V, exclude pins connected to USB bus.

Name	Parameter Description	Min.	Typ.	Max.	Unit
VCC	Supply voltage (VCC power supply, GND connects to ground)	3.0	3.3	3.6	V
VIO	VIO power supply voltage of I/O	1.7	3.3	3.6	V
ICC	Supply current when the chip is working normally	28	38	50	mA
ISLP	Supply current (USB suspend)	180	260	350	uA
VIL	Low level input voltage	0	/	0.8	V
VIH3	High level input voltage on the pin not withstanding 5V	2.0	/	VCC	V
VIH5	High level input voltage on the pin withstanding 5V	2.0	/	5.0	V
VOL	Low level output voltage (8mA sunk current)	/	/	0.4	V
VOH	High level output voltage (8mA output current)	VCC-0.4	/	/	V
RPU	Built-in pull-up equivalent resistor	30	40	60	KΩ
VPOR	Threshold voltage for power-up/power-off reset	1.9	2.2	2.5	V
VESD	ESD electrostatic withstand voltage (HBM)	4	/	/	KV

Name	Parameter Description	Min.	Typ.	Max.	Unit
VCC	Supply voltage (VCC power supply, GND connects to ground)	3.0	3.3	3.6	V

VIO	VIO power supply voltage of I/O	CH347F for lot number fifth digit < 4	1.7	3.3	3.6	V
		CH347F for lot number fifth digit ≥ 4	1.1	3.3	3.6	V
ICC	Supply current when the chip is working normally		28	38	50	mA
ISLP	Supply current (USB suspend)		180	260	350	uA
VIL	Low level input voltage	VIO=3.3V	0		0.8	V
		VIO=1.8V	0		0.5	V
VIH3	Not tolerant to high level input voltage on 5V pins	VIO=3.3V	2.0		VCC	V
		VIO=1.8V	1.3		VCC	V
VIH5	Tolerant to high level input voltage on 5V pins	VIO=3.3V	2.0		5.0	V
		VIO=1.8V	1.3		5.0	V
VOL	Low level output voltage	IOL=8mA, VIO=3.3V			0.4	V
		IOL=5mA, VIO=1.8V			0.4	V
VOH	High level output voltage	IOL=8mA, VIO=3.3V	VCC-0.4			V
		IOL=5mA, VIO=1.8V	VCC-0.4			V
RPU	Built-in pull-up equivalent resistor		30	40	60	KΩ
VPOR	Threshold voltage for power-up/power-off reset		1.9	2.2	2.5	V
VESD	ESD static tolerant voltage (manikin, non-contact)		4			KV

6.3 Timing Parameters

Test conditions: TA=25℃, VCC= 3.3V.

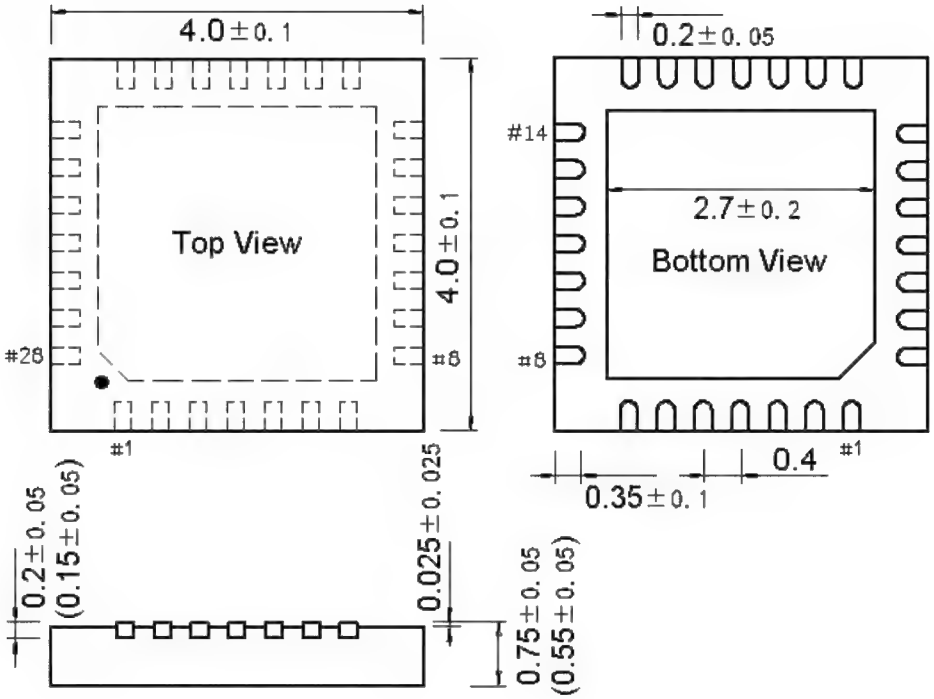
Name	Parameter Description	Min.	Typ.	Max.	Unit
tRSTD	Reset delay after power-up or external reset input	15	28	40	mS
tSUSP	Detect the USB automatic suspension time	3	5	9	mS
tWAKE	Wake-up completion time after chip sleep	0.3	0.5	2	mS

7. Package

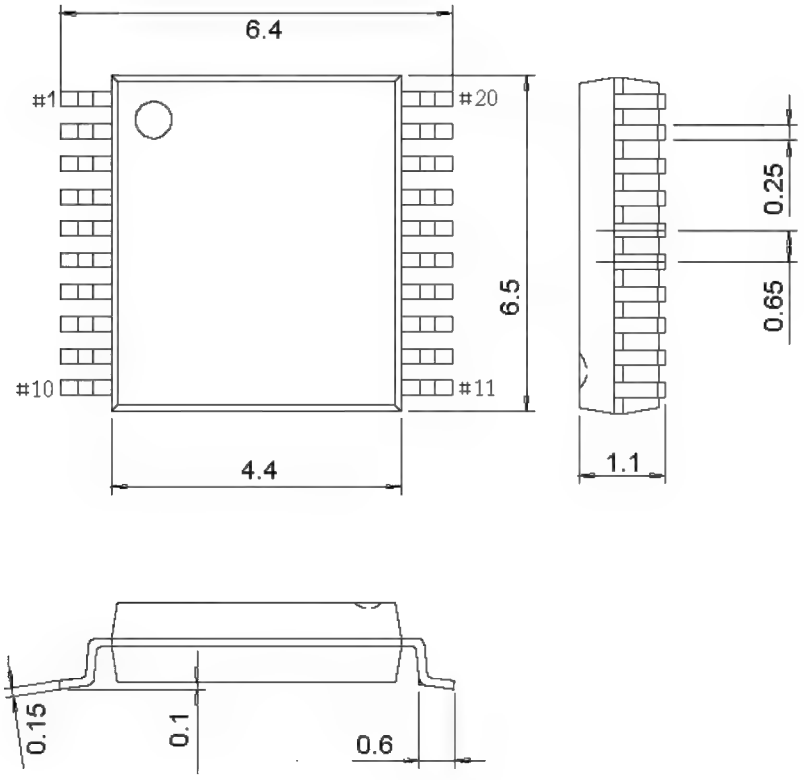
Note: The unit of dimensioning is mm (millimeter).

The pin center spacing is the nominal value without error, and the dimensional error other than that is no more than ±0.2mm.

7.1 QFN28 Package



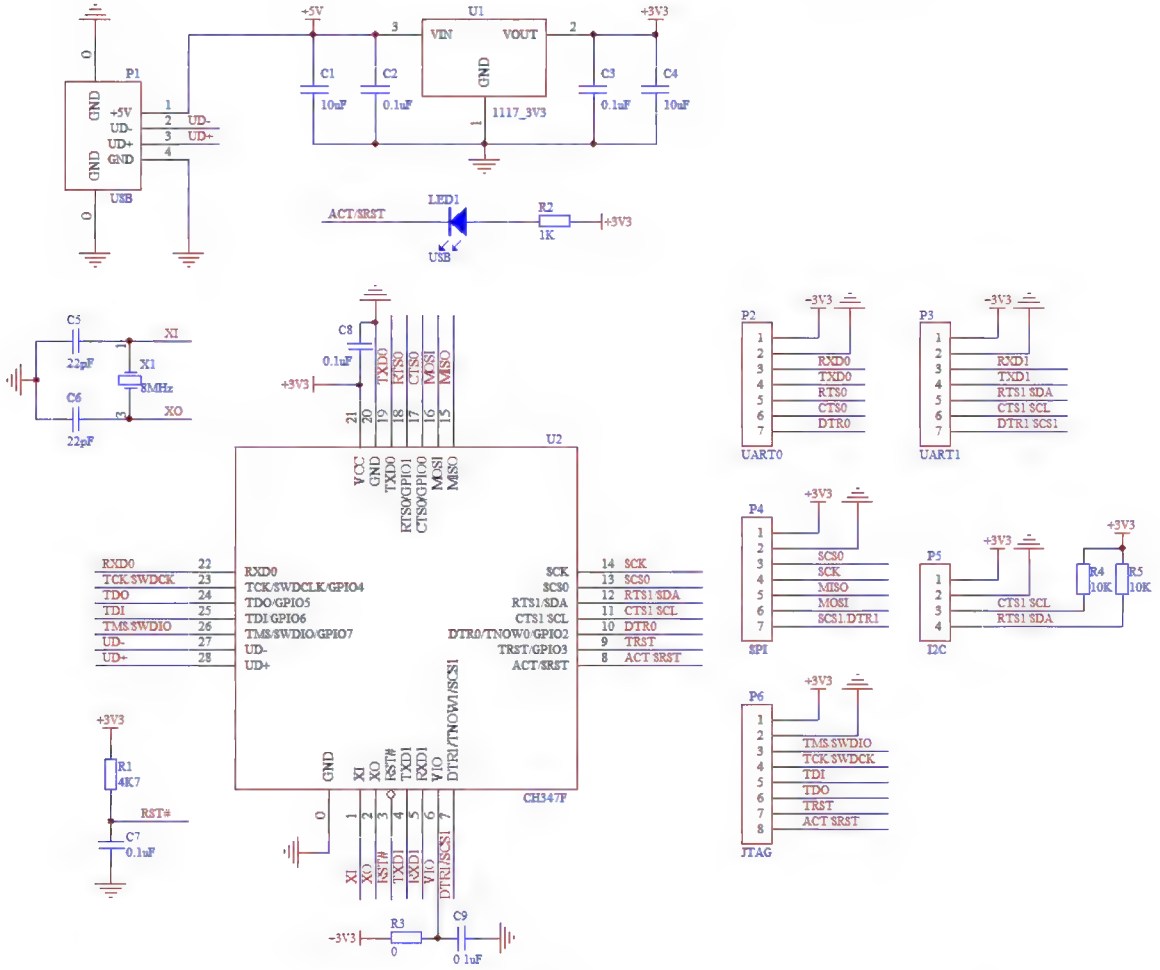
7.2 TSSOP20 Package



8. Applications

8.1 USB to Dual UART+I2C+SPI+JTAG 5-in-1

Figure 8-1 USB to dual UART+I2C+SPI+JTAG 5-in-1 reference circuit diagram



The above figure is the reference circuit diagram of USB to dual-channel high-speed serial port, 2-wire serial interface I2C, 4-wire serial interface SPI and JTAG interface realized by CH347F chip.

P1 is USB interface, and USB bus contains a pair of 5V power lines and a pair of data signal lines. Usually, the color of +5V power line is red, the black is ground. D+ signal line is green and the D- is white. The supply current provided by USB bus can up to 500mA.

P2 and P3 are TTL connection pins of serial ports, including 3.3V, GND, RXDx, TXDx, RTSx, CTSx, and DTRx pins. Can be added level conversion device (must support high baud rate), TTL to RS232, RS485, RS422 and other signal conversion.

P4 is a 4-wire synchronous serial SPI interface that includes 3.3V, GND, SCS0, SCK, MISO, MOSI, and an optional second chip selection, SCS1. P5 is a 2-wire synchronous serial I2C interface. P6 is a JTAG interface that directly connects to FPGA, CPU, and other chips.

VCC pin of CH347 inputs 3.3V power supply voltage, each power pin should be connected to a power decoupling capacitor with a capacity of about 0.1uF. In the image, C8 is power decoupling capacitors.

Crystal X1, capacitors C5 and C6 are used in clock oscillation circuit of CH347. The frequency of X1 is 8MHz± 0.4%, C5 and C6 are monolith or high-frequency ceramic capacitors with a capacity of about 22pF. R1 and C7 are optional components.

It is recommended to add ESD protection device for USB signal line. The parasitic capacitance of ESD chip

should be less than 2pF, such as CH412k.

It is recommended that peripheral interfaces (UART, I2C, SPI, JTAG) and CH347 use the same power supply. Otherwise, consider the IO pin backdown current when the power supply is separate. The VIO pin of the CH347F chip is used to provide I/O power to the I/O and RST pins, supporting 1.8V to 3.3V power source voltage, and the VIO should use the same power supply as the MCU and other peripherals.

When designing the PCB, pay attention to: the decoupling capacitor C8 gets as close to the connected power pin of CH347 as possible. The D+ and D- signal lines of the USB interface are routed close to parallel according to the high-speed USB specification to ensure the characteristic impedance, and providing ground or copper on both sides to reduce signal interference from the outside.

8.2 USB to Dual UART

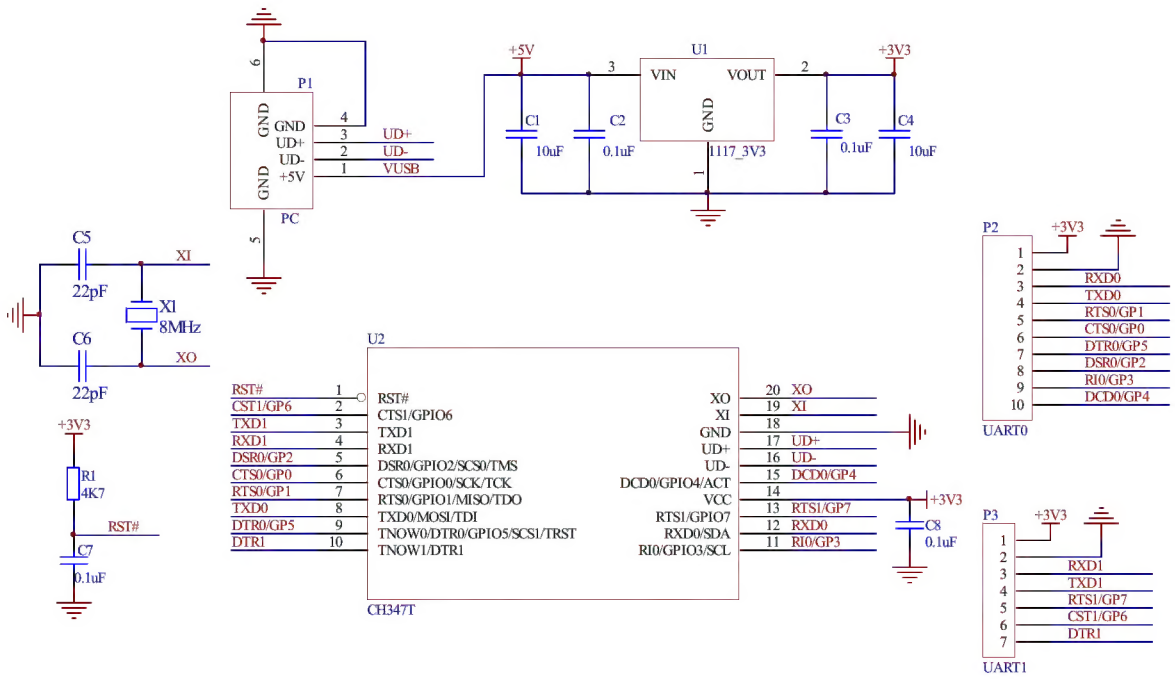
The following figure is the reference circuit diagram of the USB-to-dual-channel high-speed TTL serial port implemented by the CH347T chip, and the chip works in mode 0.

The signal lines in the figure can only be connected to RXDx, TXDx and public ground lines, and other signal lines CTSx, RTSx and DTRx can be selected according to needs, and can be suspended when not needed.

If the DTR0 is connected to a 4.7KΩ drop-down resistor, the DTR0 and DTR1 functions are switched to TNOW0 and TNOW1 respectively, indicating the transmitting status of the serial port and controlling the switch between transmitting and receiving RS485 ports.

P1 is a USB port, and P2 and P3 are TTL connection pins of 2-channel serial ports, including 3.3V, GND, RXDx, TXDx, RTSx, CTSx, and DTRx pins. Can be added level conversion device (must support high baud rate), TTL to RS232, RS485, RS422 and other signal conversion.

Figure 8-2 USB to dual UART reference circuit diagram



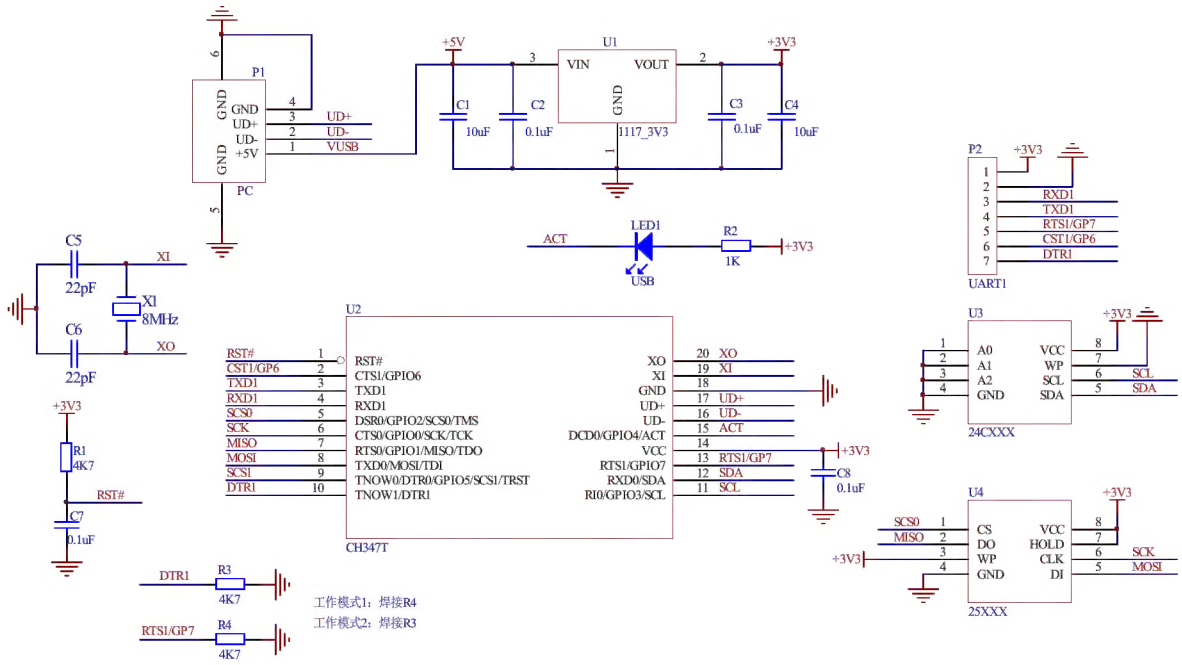
8.3 USB to SPI + I2C +UART 3-in-1

The following figure is the reference circuit diagram of the USB to high-speed single serial port and 2-wire and 4-wire synchronous serial interface implemented by the CH347T chip. R3 is removed but the resistance R4 is retained to set the chip to work in mode 1, and R4 is removed but the resistance R3 is retained to work in mode 2.

P1 is the USB port, and P2 is the TTL connection pin of the serial port, including VCC, GND, RXD1, TXD1, RTS1, CTS1 and DTR1 pins. It can add level converter to realize TTL to RS232, RS485, RS422 and other signal conversion.

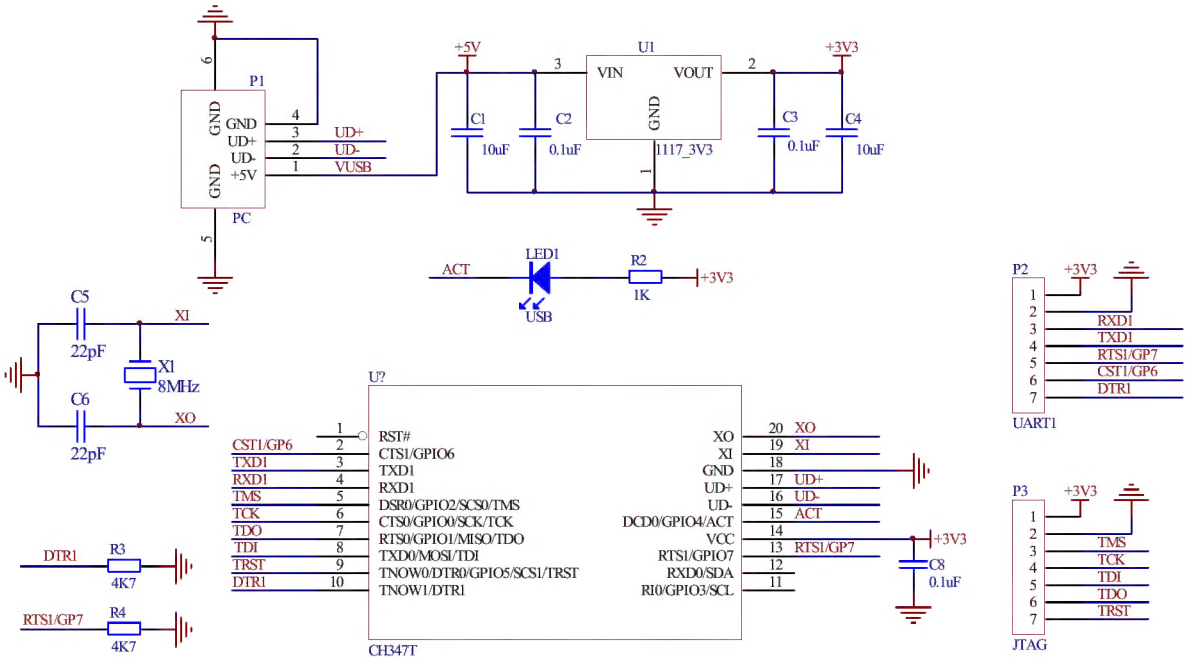
The U3 is a 2-wire synchronous serial interface I2C device. The U4 is a 4-wire synchronous serial interface SPI device. It is recommended that peripherals use the same power supply as the CH347.

Figure 8-3 USB to SPI+I2C+UART 3-in-1 reference circuit diagram



8.4 USB to JTAG + UART 2-in-1

Figure 8-4 USB to JTAG+UART 2-in-1 reference circuit diagram



The above figure is the reference circuit diagram of the USB to high-speed single UART and JTAG interface implemented by the CH347T chip. Resistors R3 and R4 set the chip to work in mode 3.

P1 is the USB port, and P2 is the TTL connection pin of the serial port, including VCC, GND, RXD1, TXD1, RTS1, CTS1 and DTR1 pins. It can add level converter to realize TTL to RS232, RS485, RS422 and other signal conversion.

P3 is a JTAG port that directly connects to FPGA and CPU chips.